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2017 Stephen and Sharon Seiden
Frontiers in Engineering & Science Workshop:

Beyond CMOS:
From Devices to Systems

June 5-6, 2017

Welcome to "Beyond CMOS" in Haifa!

CMOS scaling has been the main driver of advancements in computer capabilities over the past fifty years, while digital computing systems have been based on von Neumann architectures, where the memory and execution units are logically and physically separated. Device scaling has recently slowed down, while electrical interconnect has become both a performance bottleneck and a major source of power dissipation, which is currently the most critical limiter for technology growth. Conventional memory technologies, such as Flash, DRAM, and SRAM, are unable to keep up with market requirements for higher density and lower power.

These problems can be addressed by emerging new semiconductor devices, such as Resistive Random Access Memory (RRAM), Conductive Bridge Random Access Memory (CBRAM), Phase Change Memory (PCM), Spin-Transfer Torque Magnetoresistance Random Access Memory (STT-MRAM), memristors, 3D Xpoint, and other technologies. Since these technologies are useful both as memory cells and as novel switching circuits, they can be used to augment traditional CMOS gates while enabling novel computing systems.

This workshop brings together researchers and executives from academia and industry to discuss the many different aspects of emerging solid state technologies, including device physics, circuits, architecture, reliability, security, software, and system characteristics. These technologies provide opportunities for fundamental changes in all of these aforementioned aspects. Our workshop - "Beyond CMOS" - brings together academic and industrial professionals from different disciplines to provide perspective on the many different influences of these technologies on our world. The program includes keynote lectures in the different areas, two parallel tracks of research talks, perspective lectures, and forward looking panel sessions.

We look forward to an inspiring workshop!

Eby Friedman, Avinoam Kolodny, and Shahar Kvatinsky

Comments:

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Paper 26	
Title:	Electrical characterisation of polyaniline (PANI) based organic memristors
Author keywords:	polyaniline (PANI) based organic memristors Electrical characterisation Python voltage-current hysteresis loop
Abstract:	Polyaniline based organic memristors (PANI) with a thickness of ~50 nm have been deposited by Langmuir Schaefer procedure on a 0.2 mm thin nylon wire. The source and drain electrode were formed using a gold paste on the wire ends while the grounded silver wire immersed in the Li doped polyethylene oxide (PEO) served as a gate electrode. The memristor characteristic has been revealed by the voltage sweep in the range (-1.2V to +1.2 V) with the voltage dwell time across a structure of 15s for each 0.1 V step. The voltage-current hysteresis loop can be clearly resolved for the positive voltage sweeps. The shape and area under the hysteresis loop can be influenced by the appropriate doping of the gate electrode and polyaniline base channel. A home made measurement program in Python language has been tested on the deposited organic memristors.
Time:	May 31, 14:50 GMT

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Paper 27	
Title:	Conductivity mechanism and its time variation on polyaniline organic memristors
Author keywords:	Organic memristors Polyaniline Doping with HCl
Abstract:	Polyaniline based organic memristors have a great potential in neuromorphic structures.Both electrons and ions act as charge carriers. By applying a voltage across a PANI layer polymer undergoes reversible electrochemical oxidation and reduction. LiClO4-doped polyethylene oxide (PEO) serves as a ionic conductive polymer-solid electrolite. Most efficient improvement in electrical conductivity is still based on exposure the structure to HCl acid, under conditions that may violet the biocompatibility of the structure. Drift of the lithium ions from PEO to PANI and vice versa is exponential in nature and qualitatively explains the behavior of memristors. Influence of the exposure time on the conductivity Isd in the fiber-like memristors has been measured without the influence of the gate current.
Time:	Jun 02, 14:16 GMT

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"Memristors - Devices, Models, Circuits, Systems and Applications"

A three-day intensive training school coupled with networking opportunities

Dates: 7-9 June, 2017   **Venue:** Haifa, Israel

The recently rediscovered *memristors* have been shown to possess unique and intriguing properties, such as small size, high density, nonvolatility, and state-dependent behavior of current-voltage profiles. They are a novel class of devices that promises to revolutionize the electronics industry, and has high potential for implementing novel types of brain-inspired computing architectures and logic operations. Previous MemoCIS training schools have concentrated on the devices and their use for learning and neural networks architectures.

In this training school, we will focus more on the use of memristors for digital computing systems. We will discuss their use in memory systems as well as their use for digital processing. We will cover a wide range of aspects concerning the development and use of memristors for such systems, ranging from circuit level to architecture and software, and explore their use for different architectures and applications, such as memcomputing, memory processing units, cellular neural networks, FPGA, and more.

The training school will offer opportunities to meet some of the world-leading experts in the field and to form a multi-disciplinary network of researchers geared toward the development of memristor-based information processing systems.

The training school will start on Wednesday June 7 and finish on Friday June 9, 2017. It will take place at the Technion, Israel's leading technical institute, located in Haifa, on the Carmel Mountain, next to the Mediterranean sea. The event will immediately follow the 2017 Seiden workshop on "Beyond CMOS: from Devices to Systems" (http://tce.technion.ac.il/events/beyond-cmos/) and will start by a shared social event in Caesarea together with the Seiden workshop speakers, as a unique opportunity for the school's students to take up with leading researchers in the memristor field. The students of the training school will also present a poster at the Seiden Workshop.

The training school is open to all. It has **no registration fee**, as it is a service provided to the community, sponsored by the COST action and its members.

Financial support for travel and accommodation is available to participating COST country members. Due to budget constraints it will be limited to the most competitive applications. Application forms and instructions can be found at http://www.memocis.eu, under the Training School tab.

The training school is organized by the Technion Computer Engineering center. We will provide special rates for accommodation in selected hotels in Haifa in the training school website.
For more details, including assistance in finding appropriate accommodation, please contact Ms. Liraz Blumenkrantz Menchell (liraz@tce.technion.ac.il).

Important dates:

- Application deadline for the training school: **April 15th, 2017**
- Notification of acceptance: **April 30th, 2017**

Training Instructors:

- Alon Ascoli (Non-Linear Memristor-Based Circuits)
- Massimiliano Di Ventra (Memcomputing)
- Joseph Friedman (Logic with Spintronics)
- Pierre-Emmanuel Gaillardon (Low Power and Configurable Architectures with Memristors)
- Shahar Kvatinsky (Memristive Memory Processing Unit)
- Onur Mutlu (Memory Systems)
- Ioannis Vourkas (Logic with Memristors)

Training School Program:

Wednesday 7th June	
08:30-09:30	Registration and welcome
09:30-11:00	Opening discussion and panel session with the Seiden Workshop speakers
11:00-11:30	**Morning Break**
11:30-12:30	Introduction to memristors, Shahar Kvatinsky
12:30-13:30	Onur Mutlu, Part 1
13:30-14:30	**Lunch Break**
14:30-18:30	Onur Mutlu, Part 2
19:30-21:00	**Dinner**

Thursday 8th June	
08:30-10:15	Pierre-Emmanuel Gaillardon, "Design Opportunities of Resistive Back-End Memories: From Technology to Reconfigurable Logic"
10:15-10:45	**Morning Break**
10:45-12:30	Shahar Kvatinsky, "mMPU – memristive Memory Processing Unit – a Real In-Memory Processing System"
12:30-15:00	**Lunch Break - Trainee poster session + Lab session (in parallel)**
15:00-16:45	Joseph Friedman,
16:45-17:15	**Coffee break**
17:15-19:00	Massimiliano Di Ventra
20:00-21:00	**Dinner + Social Event**

Friday 9th June	
08:30-10:15	Alon Ascoli, "System theoretic methods for the analysis of memristor systems"
10:15-10:45	**Morning Break**
10:45-12:30	Ioannis Vourkas, "Logic Design and Computing Circuits with Memristors"
12:30-13:30	**Lunch break**
13:30-15:00	Discussion and closing remarks

Research Workshop of the Israel Science Foundation